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AK4201

Stereo Cap-less HP-Amp

GENERAL DESCRIPTION

The AK4201 is an audio stereo cap-less headphone amplifier. The AK4201 eliminates the need for large DC-blocking capacitors with a built-in Charge-pump circuit. The PSRR (Power supply Rejection Ratio) can achieve to 100dB with a built-in regulator, and it can output 2Vrms with excellent linearity when used as lineout amplifier. The AK4201 is available in tiny 12-pin USON (2.2 X 2.9mm), saving board space, cost, and component height.

FEATURE

- ☐ **Stereo Cap-less Amplifier (No DC-blocking capacitors required)**
- ☐ **High PSRR (100dB at 217Hz)**
- ☐ **Output Power:**
  - **65 mW x 2ch @ 16Ω, AVDD=PVDD=5.0V, THD+N=-40dB**
  - **30 mW x 2ch @ 16Ω, AVDD=PVDD=3.3V, THD+N=-40dB**
- ☐ **Output Noise Level: 11μVrms (Ri=20kΩ, Rf=30kΩ)**
- ☐ **Line-Out level:**
  - **2.0Vrms @ 5kΩ, AVDD=PVDD=5.0V**
  - **2.0Vrms @ 5kΩ, AVDD=PVDD=3.3V**
- ☐ **Regulator built-in**
- ☐ **THD+N**:
  - **-60 dB @ 16Ω, 50mW, AVDD=PVDD=5.0V**
  - **-60 dB @ 16Ω, 20mW, AVDD=PVDD=3.3V**
  - **-90 dB @ 5kΩ, 2Vrms, AVDD=PVDD=5.0V**
  - **-90 dB @ 5kΩ, 2Vrms, AVDD=PVDD=3.3V**
- ☐ **Low Power Shutdown Mode**
  - **0.1μA (typ)**
- ☐ **Adjustable Gain Range:**
  - **-16 dB ~ 16dB**
- ☐ **Pop noise free at power-ON/OFF**
- ☐ **Power Supply: 2.6V ~ 3.6V or 4.5V ~ 5.5V**
- ☐ **Ta: –40 ~ 85°C**
- ☐ **Package: 12pin USON (2.2 x 2.9mm, 0.5mm pitch)**

■ Block Diagram

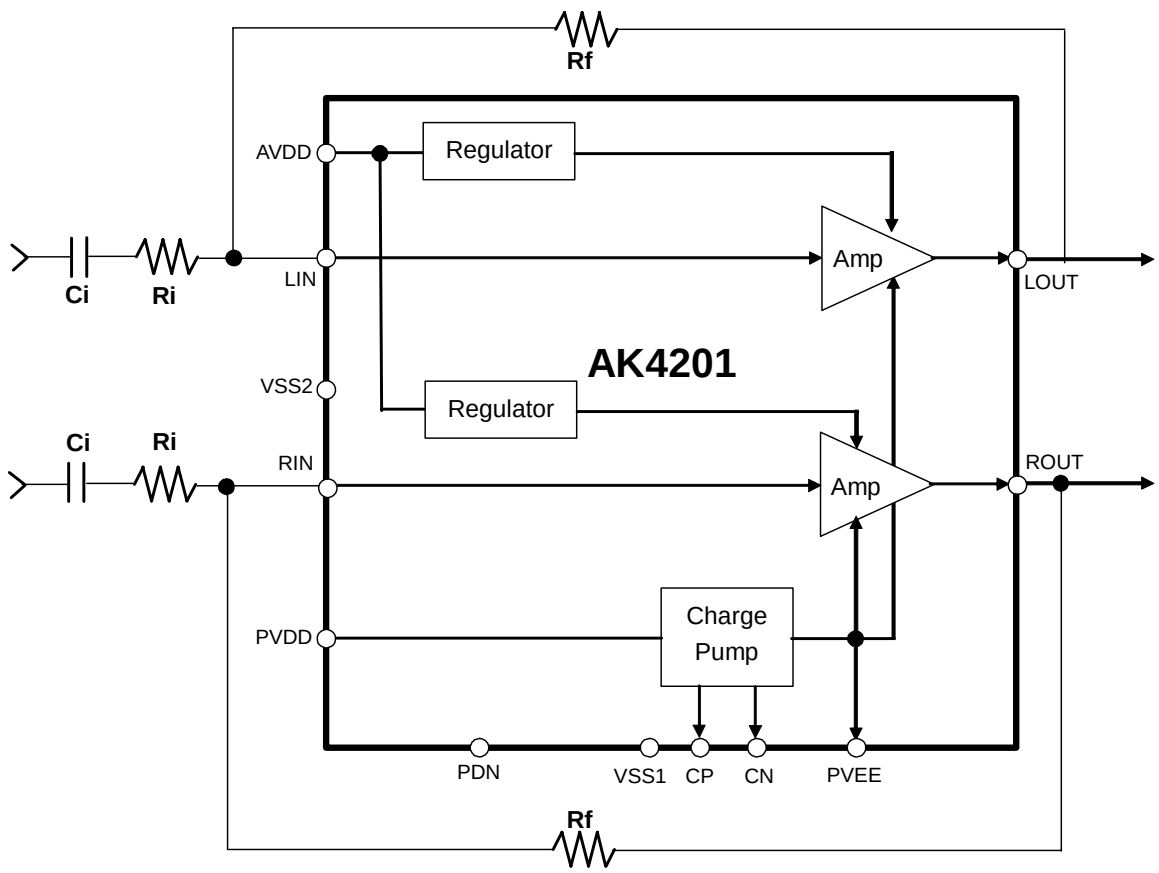
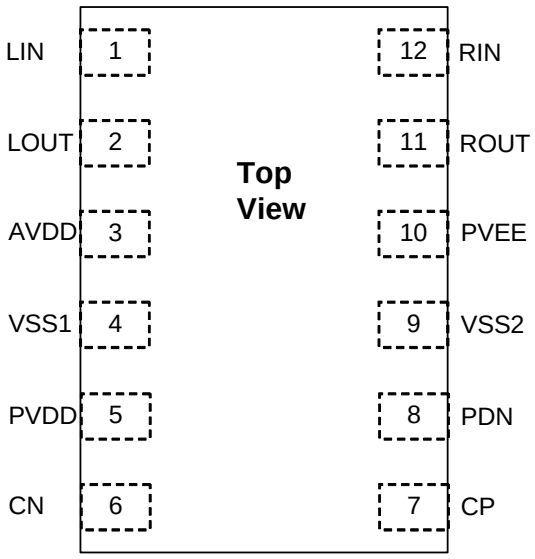


Figure 1. AK4201 Block Diagram

■ Ordering Guide

AK4201EU	–40 ~ +85°C	12pin USON (2.2mm x 2.9mm, 0.5mm pitch)
AKD4201	Evaluation board for AK4201	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	LIN	I	L-channel analog input
2	LOUT	O	L-channel analog output
3	AVDD	-	Headphone positive power supply pin, 2.6V ~ 5.5V
4	VSS1	-	Power ground
5	PVDD	-	Charge-pump positive power supply pin, 2.6V ~ 5.5V
6	CN	O	Negative charge-pump capacitor terminal pin
7	CP	O	Positive charge-pump capacitor terminal pin
8	PDN	I	Power-down mode pin "H": Power-up, "L": Power-down
9	VSS2	-	Signal ground; connect to VSS1
10	PVEE	O	Charge-pump circuit negative voltage output pin
11	ROUT	O	R-channel analog output
12	RIN	I	R-channel analog input

Note. PDN pin should not be floated.

■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

Classification	Pin Name	Setting
Analog	LIN, RIN, LOUT, ROUT	Connect Output pin to Input pin when one channel is used and the other is not used. (Example) Connect the LOUT pin to the LIN pin if Lch is not used.

ABSOLUTE MAXIMUM RATING

(VSS1=VSS2 =0V (Note 1))

Parameter		Symbol	min	max	Units
Power Supplies: (Note 2)	Analog	AVDD	–0.3	6.0	V
	Charge Pump	PVDD	–0.3	6.0	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Input Voltage (Note 3)		VIN	–0.3	(AVDD + 0.3) or 6.0	V
Ambient Temperature (powered applied)		Ta	–40	85	°C
Storage Temperature		Tstg	–65	150	°C
Maximum Power Dissipation (Note 4)		Pd	-	TBD	W

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMEND OPERATING CONDITIONS

(VSS1=VSS2 =0V (Note 1))

Parameter		Symbol	min	typ	max	Units
Power Supplies (Note 5)	Analog	AVDD, PVDD	4.5	5.0	5.5	V
	Charge Pump		2.6	3.3	3.6	
	Difference	AVDD – PVDD	-0.3	0	0.3	V

Parameter	Symbol	min	typ	max	Units
External Input Resistance	Ri	10	-	100	kΩ
External Feedback Resistance	Rf	10	-	100	kΩ
Load					
Resistance (LOUT, ROUT pins)	R_L	16	-	-	Ω
Capacitance (LOUT, ROUT pins)	C_L	-	-	300	pF
Capacitance (LIN, RIN pins)	Csum	-	-	20	pF

Note 1. All voltages are respect to ground.
Note 2. VSS1 and VSS2 must be connected to the same analog plane.
Note 3. LIN, RIN, PDN pin
The maximum value is low value either (AVDD+0.3) V or 6.0V.
Note 4. 2ch Output Power (Po, when load is 16Ω) should be less TBD W.
Note 5. The power up sequence among AVDD, PVDD is not critical. The PDN pin should be held to "L" when powered-up. The PDN pin should be set to "H" after all power supplies are powered-up. The PDN pin should be held to "L", when powered-down. Operation by the power-supply voltage from 3.6 to 4.5V is prohibited.

Note: AKEMD assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS (AVDD=PVDD=5.0V)

(AVDD=PVDD=5.0V; PDN=5.0V; Ta=25ºC; VSS1=VSS2=0V; Input Signal Frequency =1kHz; Measurement band width=10Hz ~ 20kHz; Gain=+3.5dB (Ri=20kΩ, Rf=30kΩ); Headphone-Amp: R_L =16Ω; Charge Pump Circuit External Capacitance: C1=C2= 1μF (Figure 3), unless otherwise specified)

Parameter	min	typ	max	Units
Output Power				
R_L =16Ω, 0.68Vrms Input	-	65	-	mW
THD+N				
0.68Vrms Input; Po = 65mW @ R_L =16Ω	-	–40	TBD	dB
0.60Vrms Input; Po = 50mW @ R_L =16Ω	-	–60	TBD	dB
1.33Vrms Input; Vo = 2.0Vrms @ R_L =5kΩ	-	–90	TBD	dB
S/N (Signal-to-Noise Ratio)				
R_L =16Ω (A-weighted) (Note 6)	TBD	102	-	dB
R_L =5kΩ (A-weighted) (Note 7)	TBD	108	-	dB
PSRR (Power Supply Rejection Ratio) (Note 8)				
217Hz	-	100	-	dB
1kHz	-	90	-	dB
Interchannel Isolation				
R_L =16Ω	60	80	-	dB
R_L =5kΩ	-	80	-	dB
Output Offset Voltage	-	±0.5	±5.0	mV
Start-up time (Note 9)	-	-	50	ms
Power Supplies				
AVDD + PVDD (Normal Mode; No Output)	-	4	TBD	mA
AVDD + PVDD (Power-Down Mode, PDN =0V)	-	0.1	TBD	uA

Note 6. In case of 0.68Vrms Input (Po=65mW).
Note 7. In case of 1.33Vrms Input (Vo=2Vrms).
Note 8. PSR is applied to AVDD and PVDD with 500mVpp sine wave.
Note 9. The time from PDN pin= “H” to when the AK4201 can output the data.

ANALOG CHARACTERISTICS (AVDD=PVDD=3.3V)

(AVDD=PVDD=3.3V; PDN=3.3V; Ta=25ºC; VSS1=VSS2=0V; Input Signal Frequency =1kHz; Measurement band width=10Hz ~ 20kHz; Gain=+3.5dB (Ri=20kΩ, Rf=30kΩ); Headphone-Amp: R_L =16Ω; Charge Pump Circuit External Capacitance: C1=C2= 1μF (Figure 3), unless otherwise specified)

Parameter	min	typ	max	Units
Output Power				
R_L =16Ω, 0.46Vrms Input	-	30	-	mW
THD+N				
0.46Vrms Input; Po = 30mW @ R_L =16Ω	-	-40	TBD	dB
0.27Vrms Input; Po = 10mW @ R_L =16Ω		-60	TBD	dB
1.33Vrms Input; Vo = 2.0Vrms @ R_L =5kΩ	-	-90	TBD	dB
S/N (Signal-to-Noise Ratio)				
R_L =16Ω (A-weighted) (Note 10)	92	98	-	dB
R_L =5kΩ (A-weighted) (Note 11)	100	106	-	dB
PSRR (Power Supply Rejection Ratio) (Note 12)				
217Hz	-	70	-	dB
1kHz	-	70	-	dB
Interchannel Isolation				
R_L =16Ω	60	80	-	dB
R_L =5kΩ	-	80	-	dB
Output Offset Voltage	-	±0.5	±5.0	mV
Start-up time (Note 13)	-	-	50	ms
Power Supplies				
AVDD + PVDD (Normal Mode; No Output)	-	4	TBD	mA
AVDD + PVDD (Power-Down Mode, PDN =0V)	-	0.1	TBD	μA

Note 10. In case of 0.46Vrms Input (Po=30mW).
Note 11. In case of 1.33Vrms Input (Vo=2Vrms).
Note 12. PSR is applied to AVDD and PVDD with 100mVpp sine wave.
Note 13. The time from PDN pin= “H” to when the AK4201 can output the data.

DC & SWITCHING CHARACTERISTICS

(Ta= -40 ~ 85°C; AVDD=PVDD=2.6 ~ 3.6V or 4.5 ~ 5.5V, Note 14)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	1.5	-	-	V
Low-Level Input Voltage	VIL	-	-	0.5	V
Input Leakage Current	Iin	-	-	±2	μA
Power-down (PDN pulse Width)	tPD	150		-	ns

Note 14. Apply to the PDN pin.

■ Timing Diagram

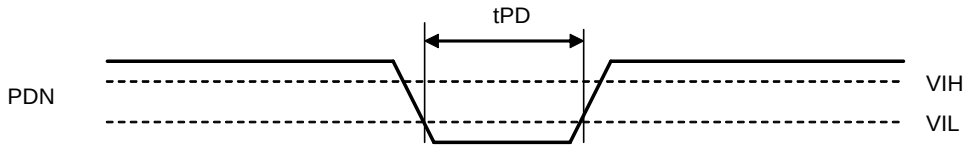


Figure 2. Power-down Timing

OPERATION OVERVIEW

■ Charge Pump Circuit

The charge pump operates by the output of a regulator which uses PVDD voltage. The negative power supply (PVEE) for headphone amplifiers is generated from internal charge pump circuit. The external capacitors are showed in Figure 3. Low ESR (Equivalent Series Resistance) capacitors (more than –35% difference including temperature characteristics and piece to piece variations) are recommended for C1 and C2.

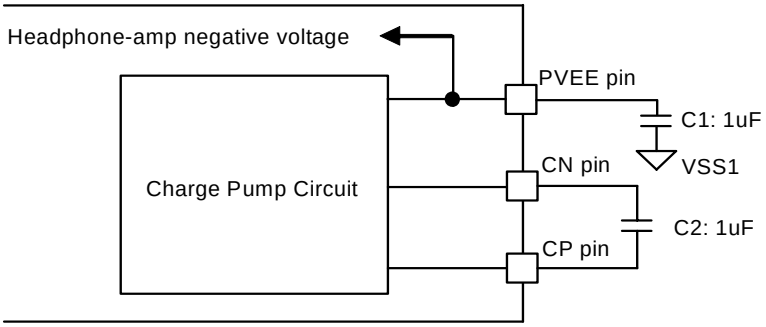


Figure 3. Charge Pump Circuit External Capacitor

■ Headphone-Amp (LOUT/ROUT pins)

Power supply voltage for headphone amplifiers is supplied by a regulator for positive power and a charge-pump for negative power. The positive power supply for Charge pump is generated from the output of a regulator which is driven by PVDD. The headphone amplifier output is single-ended and centered on VSS1(0V). Therefore, a capacitor for AC-coupling can be removed. The minimum load resistance is 16Ω. The output impedance is 20Ω (typ) when powered-down.

■ Power-Up/Down Sequence

The PDN pin must keep "L" until all power supply pins (AVDD, PVDD) are supplied, and must be set to "H" after all powers are supplied.

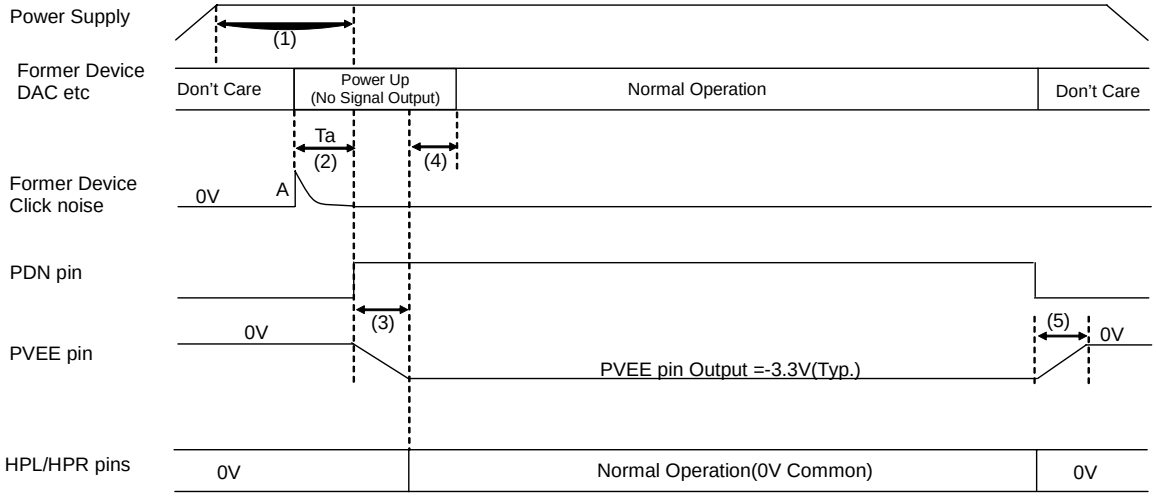


Figure 4. Power-up/down Sequence example

(1) The interval from power Up to PDN pin = "L" → "H"
"L" time of 150ns or more is needed to reset the AK4201.
The power should be ON in state of the PDN pin = "L". The PDN pin should be set to "H" after power supply (AVDD, PVDD) are ON.

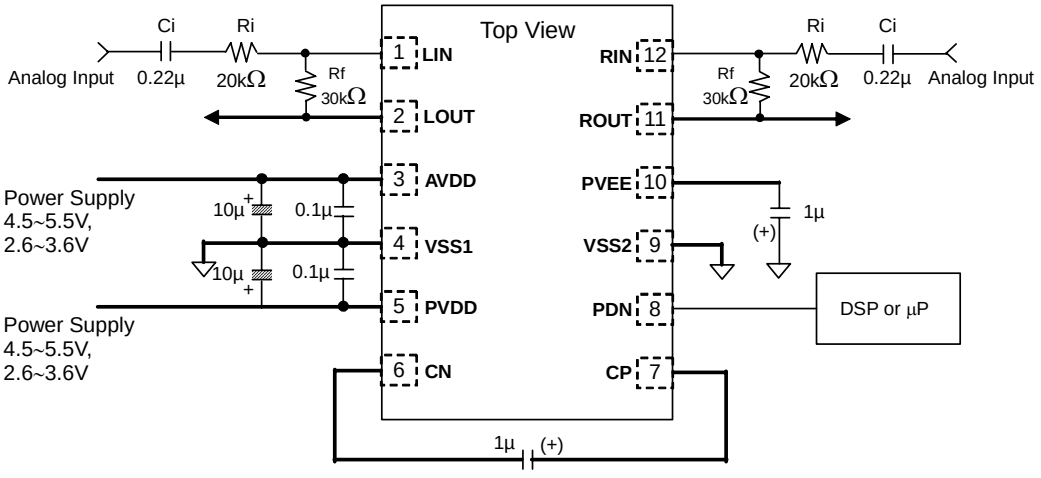
(2) The interval from former device of the AK4201(DAC etc) power up to the PDN pin = "L" → "H"
The former device of the AK4201 should be powered up with no output (MUTE). When step wave which generated by former device is output (an instant change of DC offset), HPF response wave will occur at "A" period of the Figure 4, according to the AK4201 input coupling condenser (Ci) and input resistor (Ri). In order to avoid click noise, "Ta" wait time is needed after former device output.
Ta calculation example: (in the case of Ci =0.22uF, Ri = 20kΩ)
τ=0.22u * 20k = 4.4ms
Ta =τ* 7.6 = 33ms
(When noise level by former device= 2V, response wave level= 1mV. 7.6*τ is needed)
If waiting time is not sufficient, click noise maybe occur, but no problem for later working.

(3) 50ms (max.) later, after the PDN pin went to "H", the AK4201 will be in normal operation mode and click noise is decreased. In this interval (50ms), the former device should be MUTE.

(4) The former device should starts outputting the signal after the AK4201 starts Normal Operation. If click noise is generated by former device when MUTE is canceled, it will be output from the AK4201.

(5) The PDN pin = "L". LOUT/ROUT pins short to VSS1 with 20Ω(typ.). After 50ms (max.), the PVEE pin will be 0V according to a capacitor which connected to PVEE and internal resistance (typ. 17.5kΩ). The AK4201 can be powered up again after 150ns or more from the PDN = "L".

SYSTEM DESIGN



Note:

1. The PDN pin should be held to "L" when powered-up. The PDN pin should be set to "H" after all power supplies are powered-up. When power-down the AK4201, the PDN pin should be held to "L".

Refer to "Power-Up/Down Sequence" to avoid pop noise when power-up/down the AK4201.

1) Power-Up
The power should be ON when the PDN pin = "L". The PDN pin should be set to "H" 150ns after all power supplies (AVDD, PVDD) are ON. 150ns "L" time or more is needed to reset the AK4201.

2) Power-Down
The AK4201 should be powered-down when the PDN pin = "L".

2. 1uF~2.2uF ceramic capacitors (±35% including temperature characteristics and piece-to-piece variations)should be connected to between the Cp and Cn pins, and the VSS1 and PVEE1 pins.

3. Both lines from the LIN pin and RIN pin to each Input resistance Ri and feedback resistance Rf should be short as possible.

4. A capacitor should be connected to the each LIN and RIN pin for AC coupling.

PACKAGE

12pin USON (2.2mm x 2.9mm, 0.5mm pitch)

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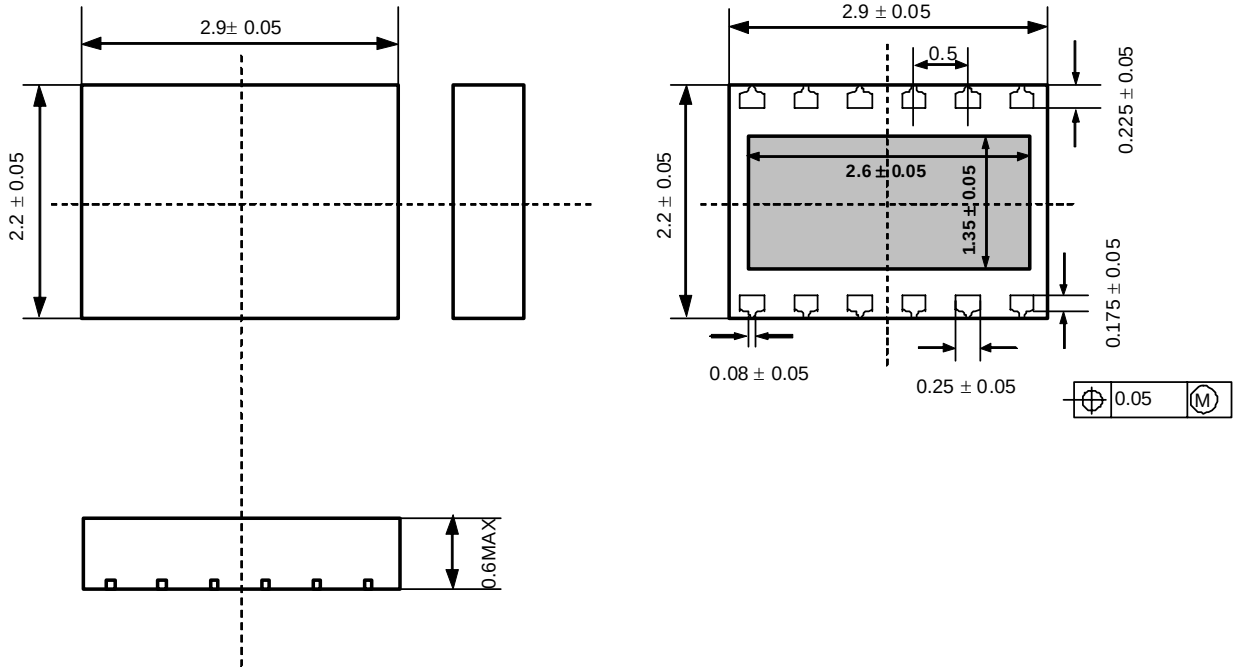
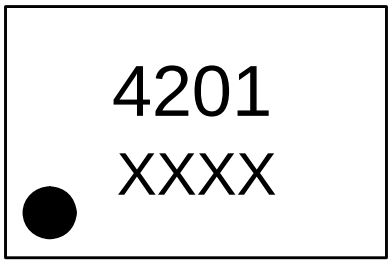


MARKING



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